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COTS in Space: Constraints, Limitations and Disruptive Capability

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Motivation

- Performance of commercial electronic integrated components (COTS ICs) with regard to their space qualified counterparts is increasingly attractive for space applications

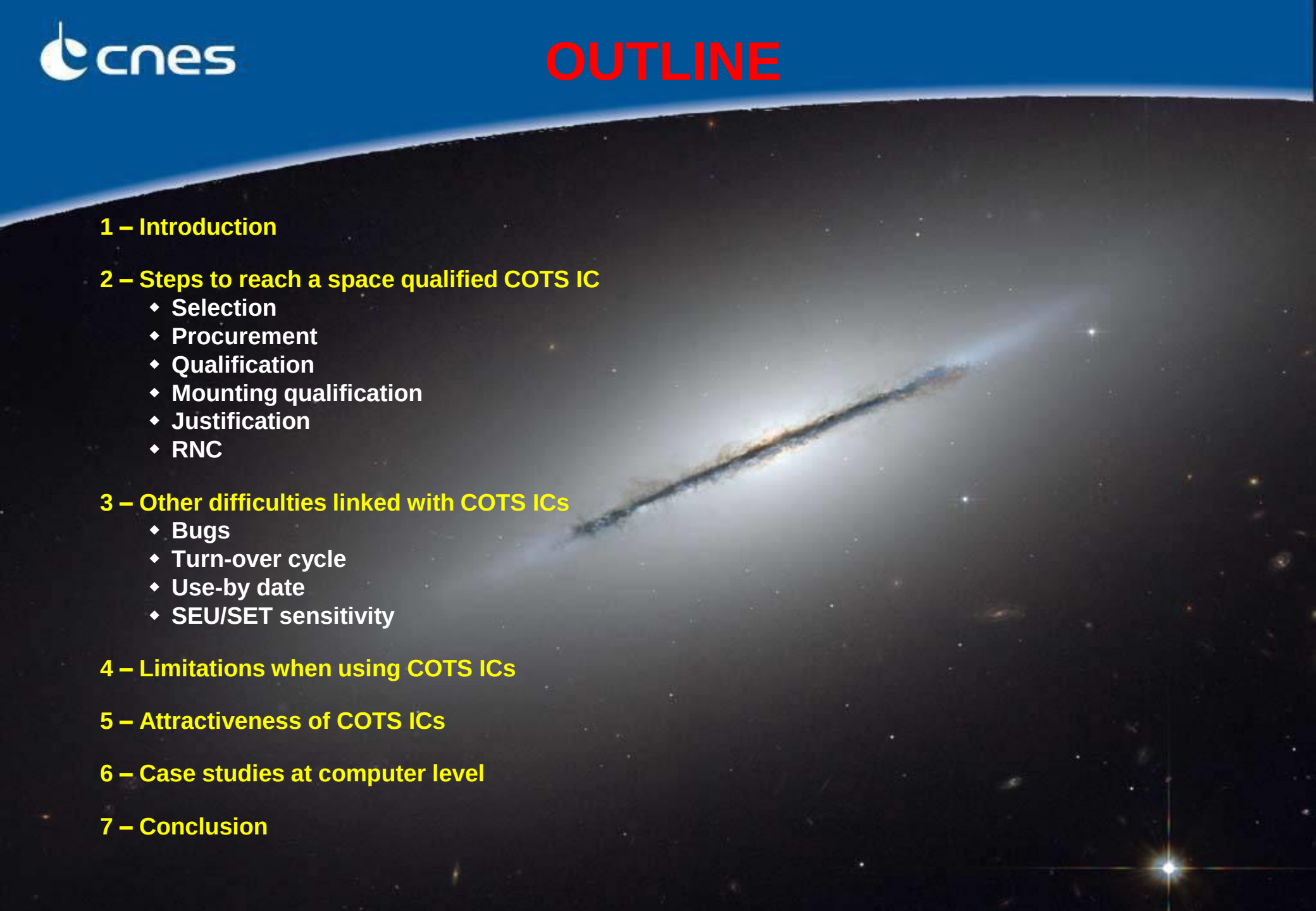
- But COTS components have to successfully pass different steps before being accepted for flying, in particular in the constraining space environment…

- … generating large cost / planning overheads!

=> Clarification of the "myth": COTS ICs are cheaper than HiRel / space qualified ICs

=> Are COTS ICs really attractive for space applications?

OUTLINE



1 – Introduction

2 – Steps to reach a space qualified COTS IC
- Selection
- Procurement
- Qualification
- Mounting qualification
- Justification
- RNC

3 – Other difficulties linked with COTS ICs
- Bugs
- Turn-over cycle
- Use-by date
- SEU/SET sensitivity

4 – Limitations when using COTS ICs

5 – Attractiveness of COTS ICs

6 – Case studies at computer level

7 – Conclusion

Acronyms

CNES	*Centre National d'Etudes Spatiales, the French Space Agency*
ESA	*European Space Agency*

ADC	Analog to Digital Converter
ASIC	Application Specific Integrated Circuit
Cmd	Command
Cntl	Control
COTS	Commercial Off-The-Shelf
CPU	Central Processing Unit
DPA	Destructive Physical Analysis
DSP	Digital Signal Processor
EDAC	Error Detection And Correction
FM	Flight Model
FT	Faut-Tolerant
HAST	Humidity Accelerated Stress Test
HiRel	High Reliability
HSSL	High Speed Serial Link
HW	Hardwire
IC	Integrated Circuit
I/O	Input/Output
LAT	Lot Acceptance Test
MMIC	Monolithic Microwave Integrated Circuit
PF	PlatForm (of a satellite)
PL	PayLoad (of a satellite)
SW	Software
SEM	Scanning Electron Microscopy
SerDes	Serializer/Deserializer
SSMM	Solid State Mass Memory
Tx/Rx	Transmitter/Receiver
µP	MicroProcesseur
wrt	With Regard To
MBU	Multiple Bit Upsets
SEE	Single Event Effect
SEFI	Single Event Functional Interrupt
SEL	Single Event Latch-up
µSEL	Micro latch-up
SET	Single Event Transient
SEU	Single Event Upset
TID	Total Ionizing Dose

Introduction

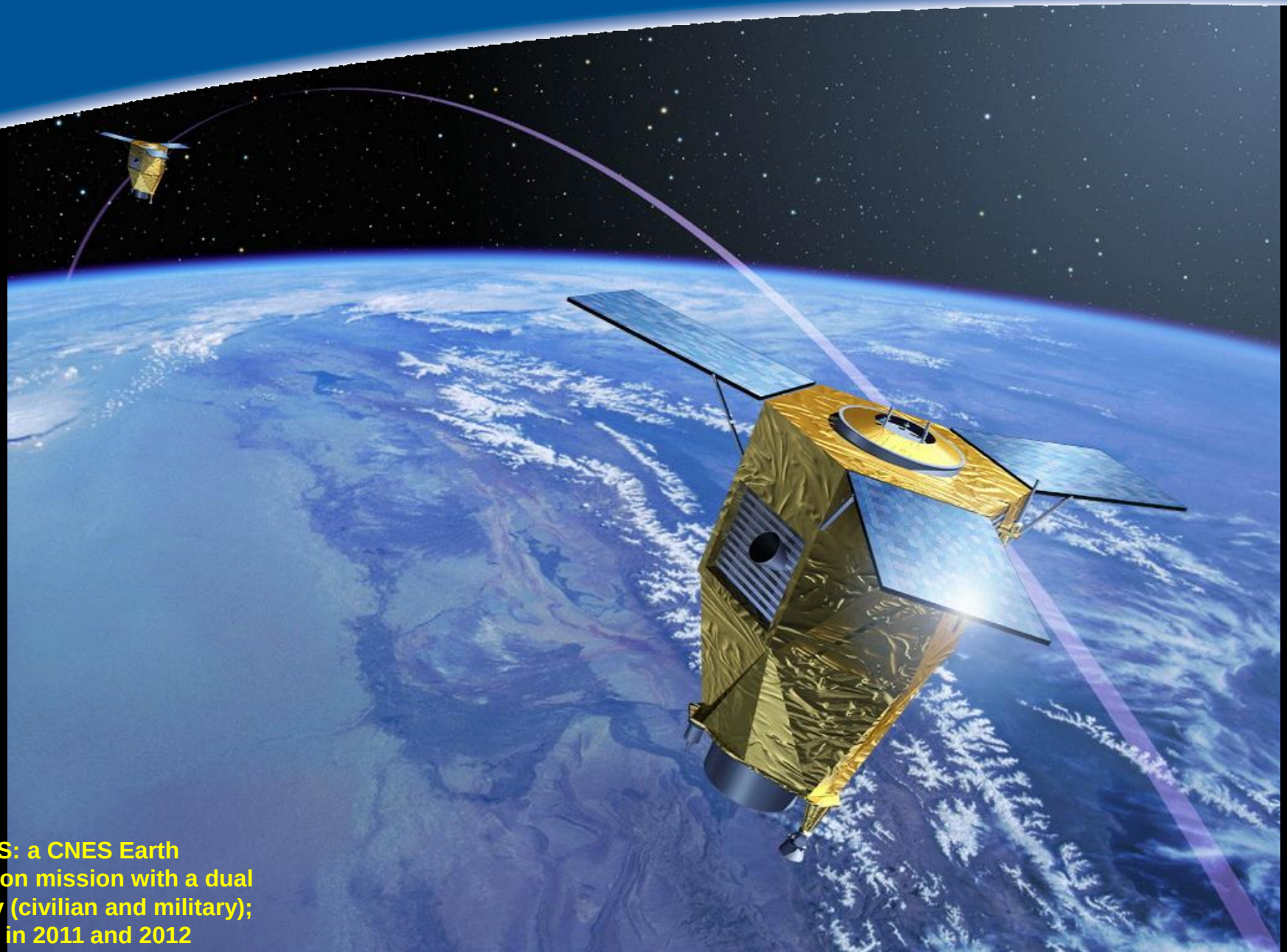
- Some COTS ICs have always been used from time to time
  - DSP, microcontrollers, memories, ADC, …

- The space industry has compensated for the reduction of the HiRel ICs market thanks to space qualified ASICs and HiRel MMICs

- Although the use of COTS components is very limited at the moment, their attractiveness seems continuously increasing thanks to their higher and higher performances

=> COTS use in space applications is possible but costly, and must respect some contraints

2 – Steps to reach a space qualified COTS IC



PLEIADES: a CNES Earth observation mission with a dual capability (civilian and military); launched in 2011 and 2012

Presentation of the COTS methodology

Few remarks

=> The COTS methodology is illustrated by the qualification of the G-Link components from Agilent, a SerDes / HSSL used in CNES Pleiades satellite

- ***G-Link on Pleiades is a typical and complete example of an occasional use of a commercial component due to its high performances***

=> The word "qualification" is used because more understandable, but the exact word for Quality Experts is "validation" (=> "quality validation")

=> The uncertainty to succeed during the qualification steps must be kept in mind

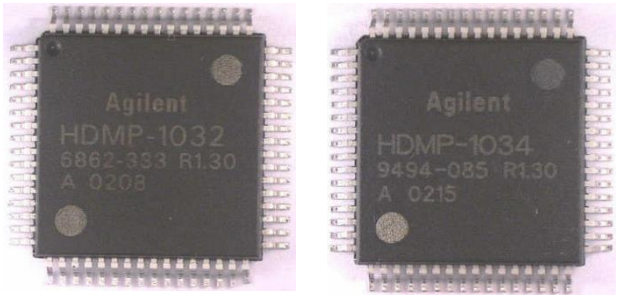
- ***For a given project, attractive COTS could not be selected only wrt that issue***

Selection

- **Selection step**
  - Done in close collaboration between the Design team and the Product Assurance team
  - Choose as a priority the "most mature components from major suppliers" => usually the most reliable and the longest life cycle

- **Results of the Pleiades study**

=>
  - There was no space qualified component compliant with the Pleiades HSSL need
  - To reduce the risk to fail during the qualification process, four COTS were evaluated
    - G-Link from Agilent (HDMP-1032 Tx + HDMP-1034 Rx)
    - VSC7212 from Vitesse Semiconductors
    - FC106 from STMicroelectronics
    - DS92LV16 from National Semiconductors
    - DS90CR21X / 28X from NS was partially taken into account
  - Final result: choice of the G-Link



HDMP-1032 (Tx) and 1034 (Rx)

Procurement

- **Procurement step**
  - A single **lot of components** (single date-code) because some qualification tests are destructive so they are performed on a sample
  - The knowledge, the quality and the control of the **procurement chain** is important to keep an efficient **traceability** and to avoid **counterfeit** parts
    - Up to 20 % of IC lots from non official distributors are counterfeit
      - e.g. ICs which couldn't reach the datasheet perfo (freq, pw consumpt° , …) or the required reliability level, etc.

      => Overcost due to electronic counterfeit ICs at world level, all domains included, is roughly about 100 G$
  - Usually a **strategic stock** is done to face short life cycle of COTS

- **G-Link result(s)**
  - Strategic stock including **1000 Tx** and **1000 Rx**
  - It covered about **twice** the needs for Pleiades, to allow other projects to use these components without having to replay a **long** and **costly** qualification procedure

Lot qualification (1/2)

- **Selection of tests wrt project**
  - The qualification tests depend on the "Quality Assurance" level of the project
  - On the one hand, COTS must be evaluated and qualified before being used in space projects: "use as is" approach is extremely inadvisable
  - On the other hand, tests to apply have to be adapted, and possibly reduced, with regard to the selected component and mission requirements to find the best trade-off between cost and quality

- **Tests involved in the lot qualification step / "Lot Acceptance Tests" (LAT)**
  - A - Tests that are fairly conventional in all types of embedded applications, e.g.:
    - electrical characterization at three temperatures
    - construction analysis – "Destructive Physical Analysis" (DPA)
    - life-test => long-term reliability test
    - screening test / burn-in => to pass over the first part of the 'bath curve' (to avoid infant mortality)
    - thermal cycling tests (due to differential dilatation coeff between silicon and plastic packages)
    - ON/OFF power cycling tests for some missions: Earth observation payloads can require 100,000 power cycles for power optimisation and, at this time, there is very little feedback on the behaviour of plastic packaged components with regard to this way of operating

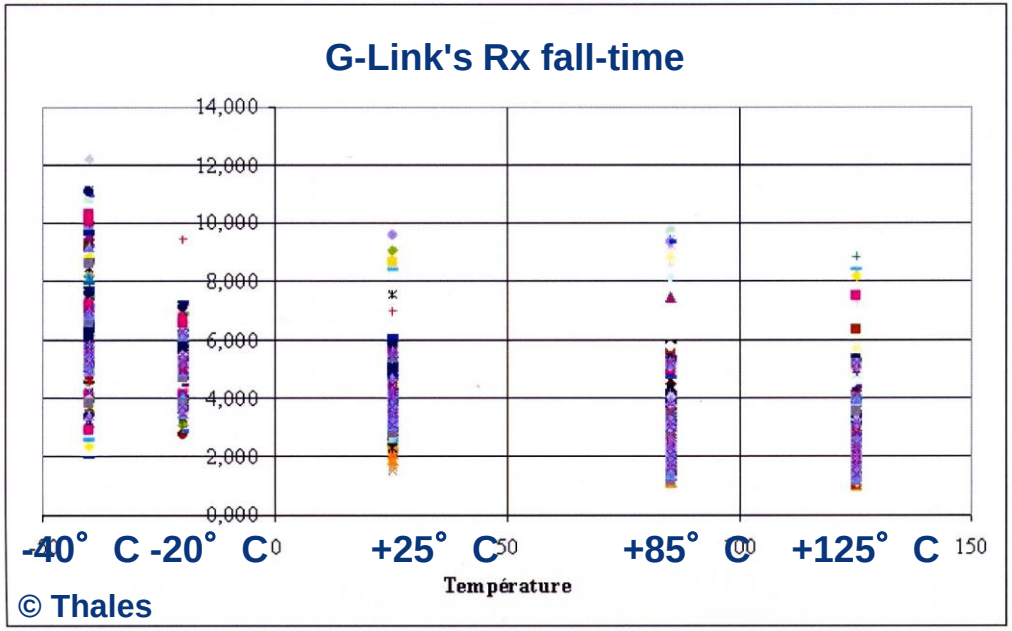
Lot qualification (2/2)

- Tests involved in the lot qualification step (cont')
  - B - Tests linked to some problems common to both HiRel and COTS, but to which COTS are more subject to, e.g.:
    - damp heat tests (e.g. HAST "Highly Accelerated Stress Tests") specific to plastic packages
    - if required, some risk analysis are done to define mitigation actions, e.g.:
      - risk of 'whiskers'
      - risk of 'purple plague'
  - C - Tests specific to the space domain, related to the environment or mission requirements, e.g.:
    - TID (Total Ionising Dose)
    - SEL (Single Event Latch-up)
    - SEU (Single Event Upset)
- G-Link result(s)
  - See illustrations in next slides

Some illustrations for "Electrical characterization", "DPA", "risk analysis" and "TID characterization"

G-Link qualification tests were mainly done by CNES and "Thales Communications & Security" High-Reliability Laboratory; some complementary tests were done by EADS Astrium and by Thales Alenia Space

Electrical characterization

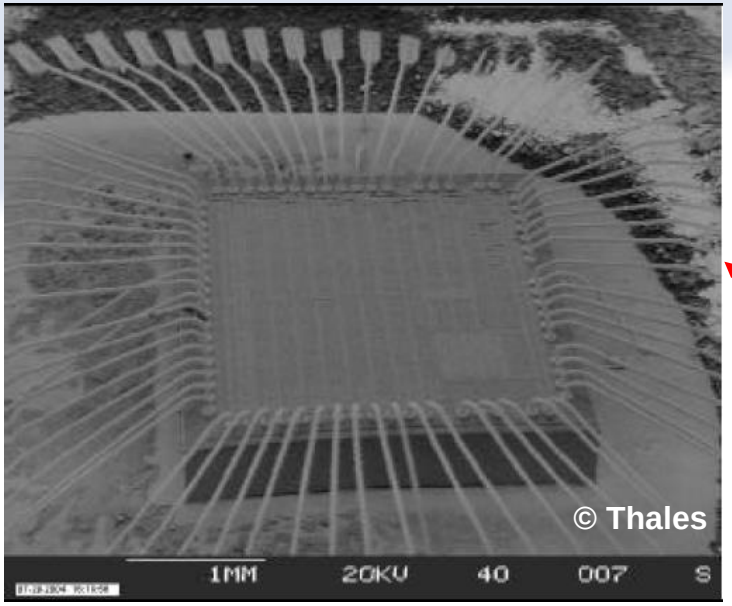


Tests at 5 t° (50 pairs) to check the compliance with the datasheet and to analyse the homogeneity of the lot

DPA

Check quality of manufacturing

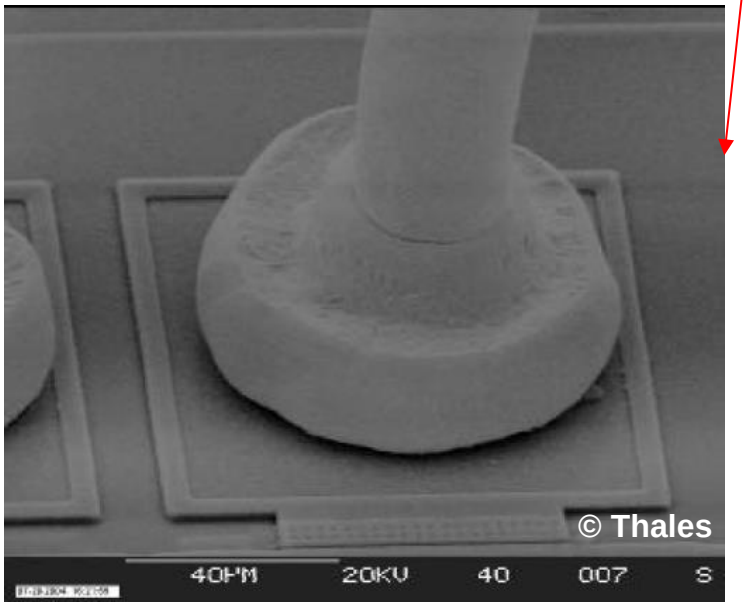
Contribution from:
G. Perez (CNES - DCT/AQ/LE)



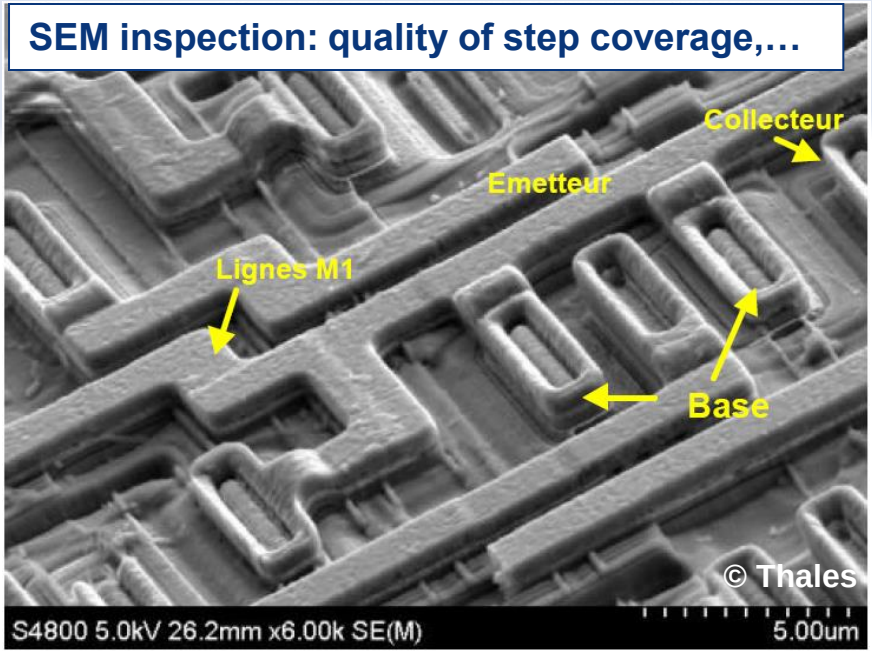
G-Link

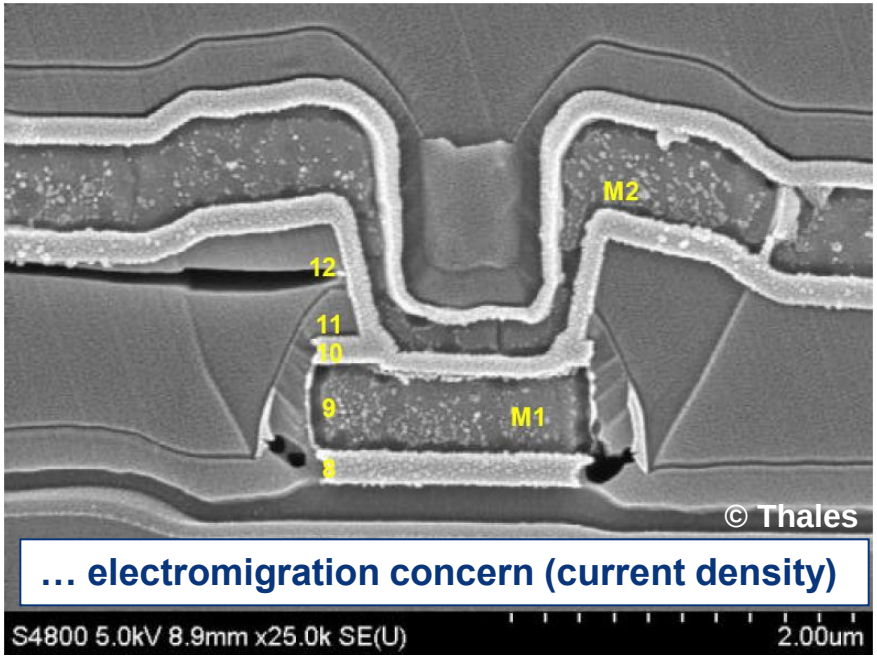
At the assembly level:
- **die attach**
- **wire bonding**

At the die level:
- **surface view**
- **cross-section detail**



SEM inspection: quality of step coverage,…



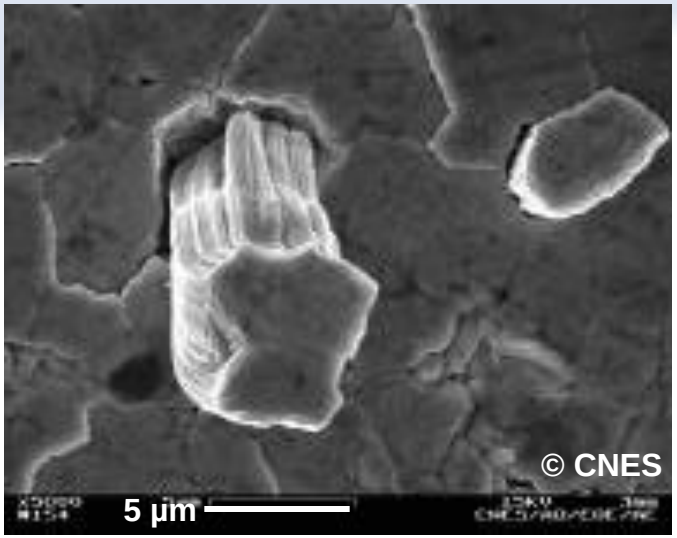


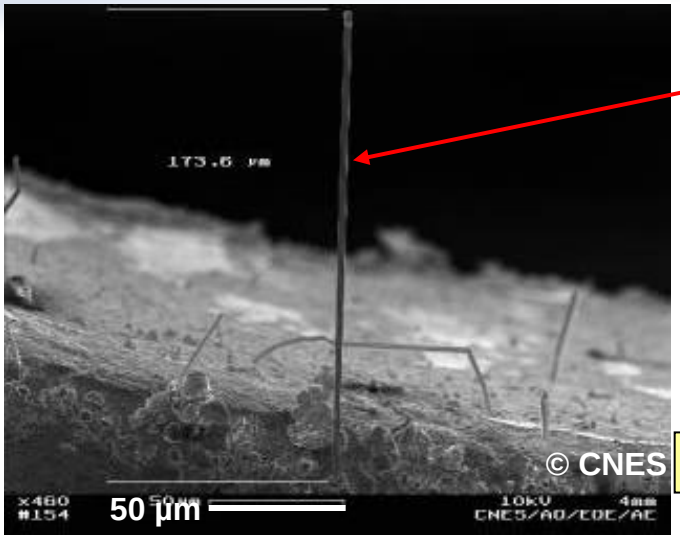
… electromigration concern (current density)

Exemples of defects during DPA

Contribution from: G. Perez
(CNES - DCT/AQ/LE)

Whiskers





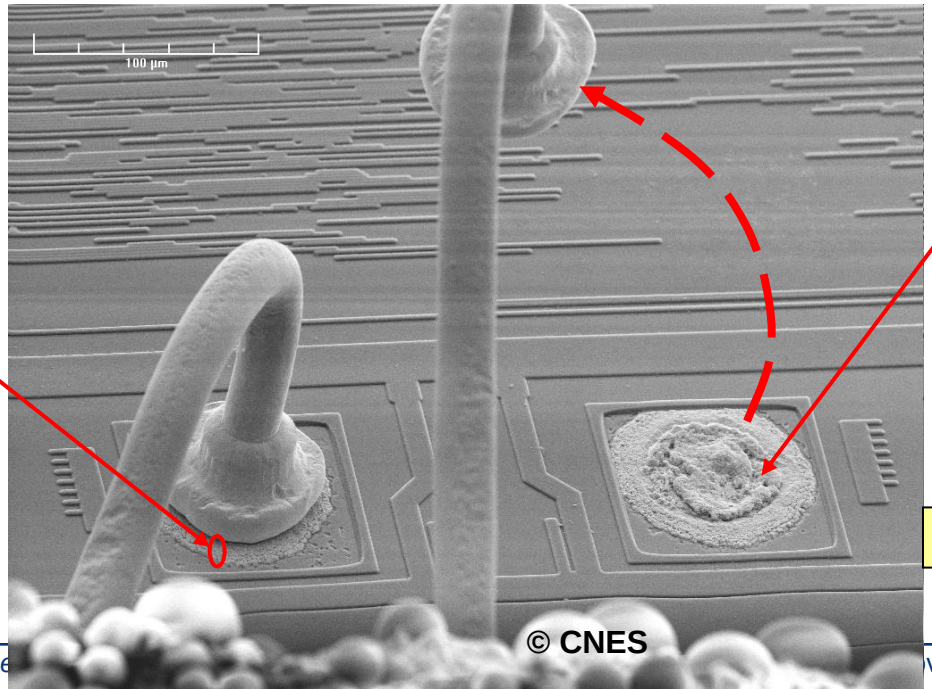
Whiskering effect that can lead to short-circuit (e.g. on a CNES Spot 4 equipment)

Favoured by pure Tin lead finish (leadless)

REJECTED STOP

Not G-Link components

Purple plague



Purple plague: intermetallic growths that can lead to de-bonding

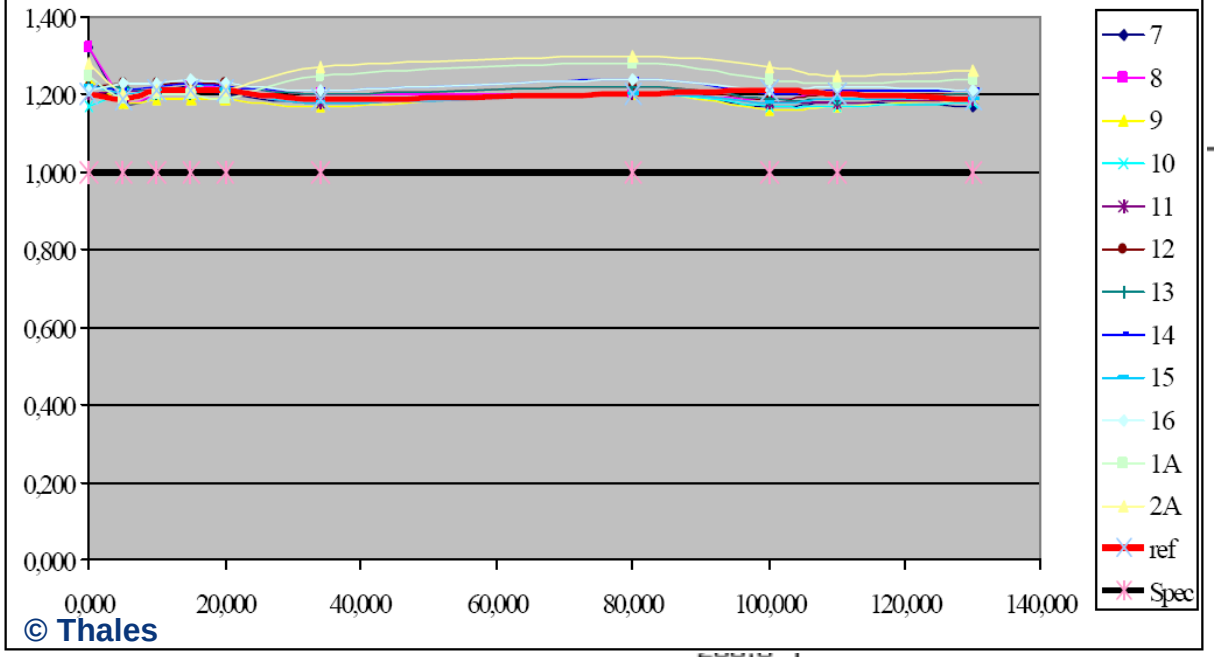
Favoured by bonding process: interface between gold (bond) and Alu (pad) under thermal constraints

REJECTED STOP

TID characterization

G-Link component in bipolar techno

Vop

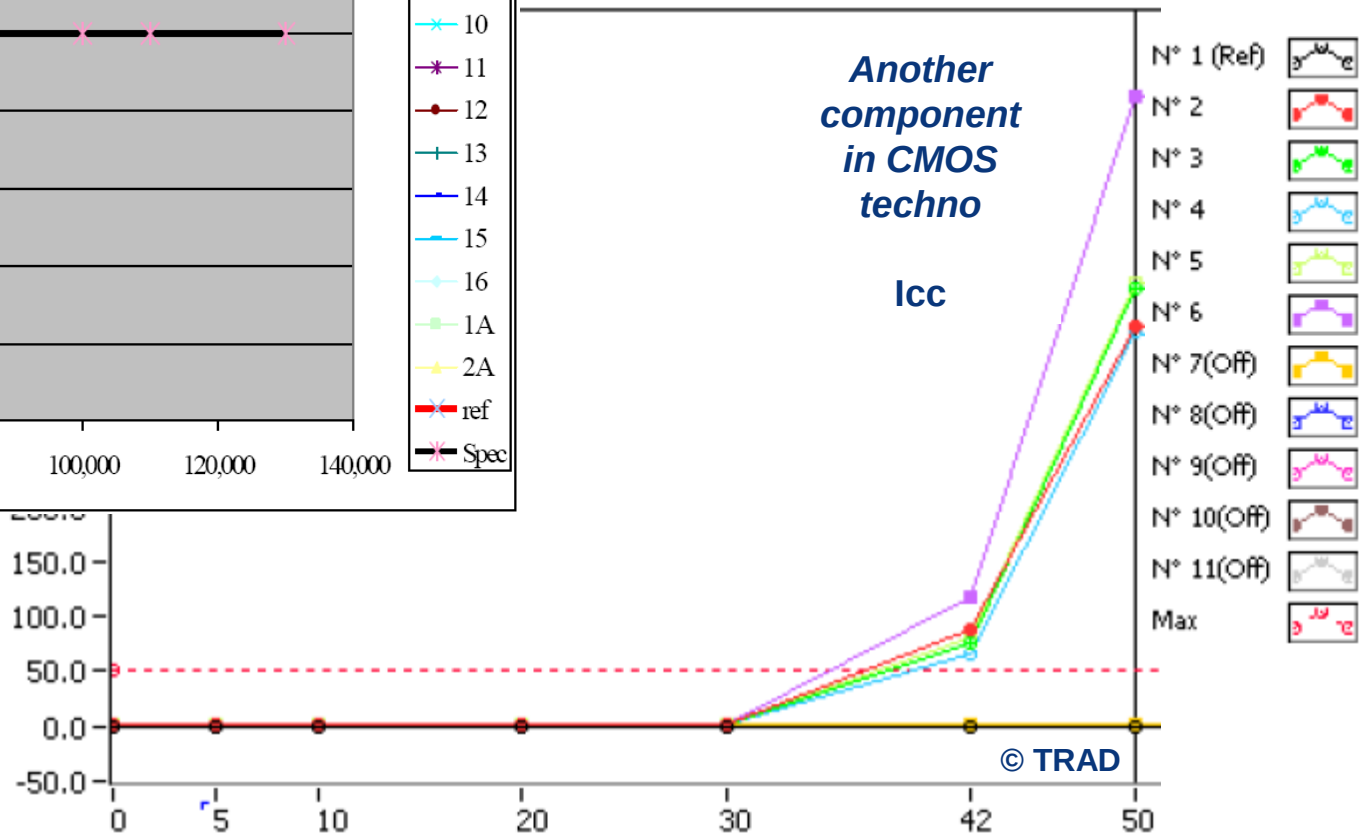


© Thales

Total ionizing dose tests (10 pieces for the G-Link)

Another component in CMOS techno

Icc



© TRAD

Mounting qualification

Contribution from: T. Battault (CNES - DCT/AQ/MP)

- **The mounting on a PCB of each type of package has to be qualified, the associated know-how for a given company being described in its "Process Identification Document" (PID)**
- **PID is a qualification flowchart including: facilities and tools (1), staff certification method, products and packages, mounting config. (2), materials, soldering process, etc.**

  (1) Soldering oven (vapour phase machine), … (2) Glued or not, PCB varnished or not, …

  - **Verification tests of the PID include: vibration testing, thermal cycling (due to the differential dilatation coeff between PCB and package materials), visual inspection and micro-sectioning**

➢ ***E.g. of COTS IC mounting qualification status in 2012 in the European space community***

- ✓ ***Already qualified: up to e.g. 64-pins plastic PQFP***
- ✓ ***Qualification started in 2012: plastic PBGA-240, ceramic CGA-1144 - 1 mm pitch (Virtex 4)***

Nota: CGAs require heavy industrial facilities and method teams (only 3 companies qualified in France)

(PQFP = Plastic Quad Flat Pack)
(PBGA = Plastic Ball Grid Array)
(CGA = Column Grid Array, requiring an interposer)

- **G-Link result(s)**
  - **It was required to qualify the mounting of its PQFP-64 package for each user companies**

Justification

- At the end of the selection step, a "Justification Document" (JD) is issued; then it is updated all along the qualification process
  - The JD is an important document summurazing in a few pages the ID of the qualified component, i.e. a synthesis of its essential informations and test plans

- G-Link result(s)
  - Actions plan
    - e.g. "Risk = Purchasing will become not possible in a short term due to an obsolescence alarm"
      => "Actions = To be secured by a stock"
      => "Status = To be done" (then "Status = OK")
  - General informations
    - Few informations linked with the qualification process, e.g.: die techno., packaging techno., marking, t° range, manufacturing sites, etc.
  - Supporting data set
    - e.g.: ESD sensitivity, screening flow, radiation test (with quantity of tested ICs, conditions, results, dates), electrical tests, ageing tests, outgasing tests, etc.

RNC concerning COTS ICs

- The RNC (CNES Normative Referential) is a set of documents describing all the norms the space industry has to comply with to provide spacecrafts / subset, or to launch / operate spacecrafts

- The RNC covers the main domains included in the space know-how
  - Management; e.g.: configuration managmt, cost and delay mastering, risk managmnt
  - Product Assurance; e.g.: Quality Assurance, dependability, EEE components
  - Engeniering; e.g.: system engeniering, electronic engnr, mechanical engnr, ground operation engnr, launch engnr
  - Regulation; e.g.: launch safety, space debris, manned flight, planetary protection

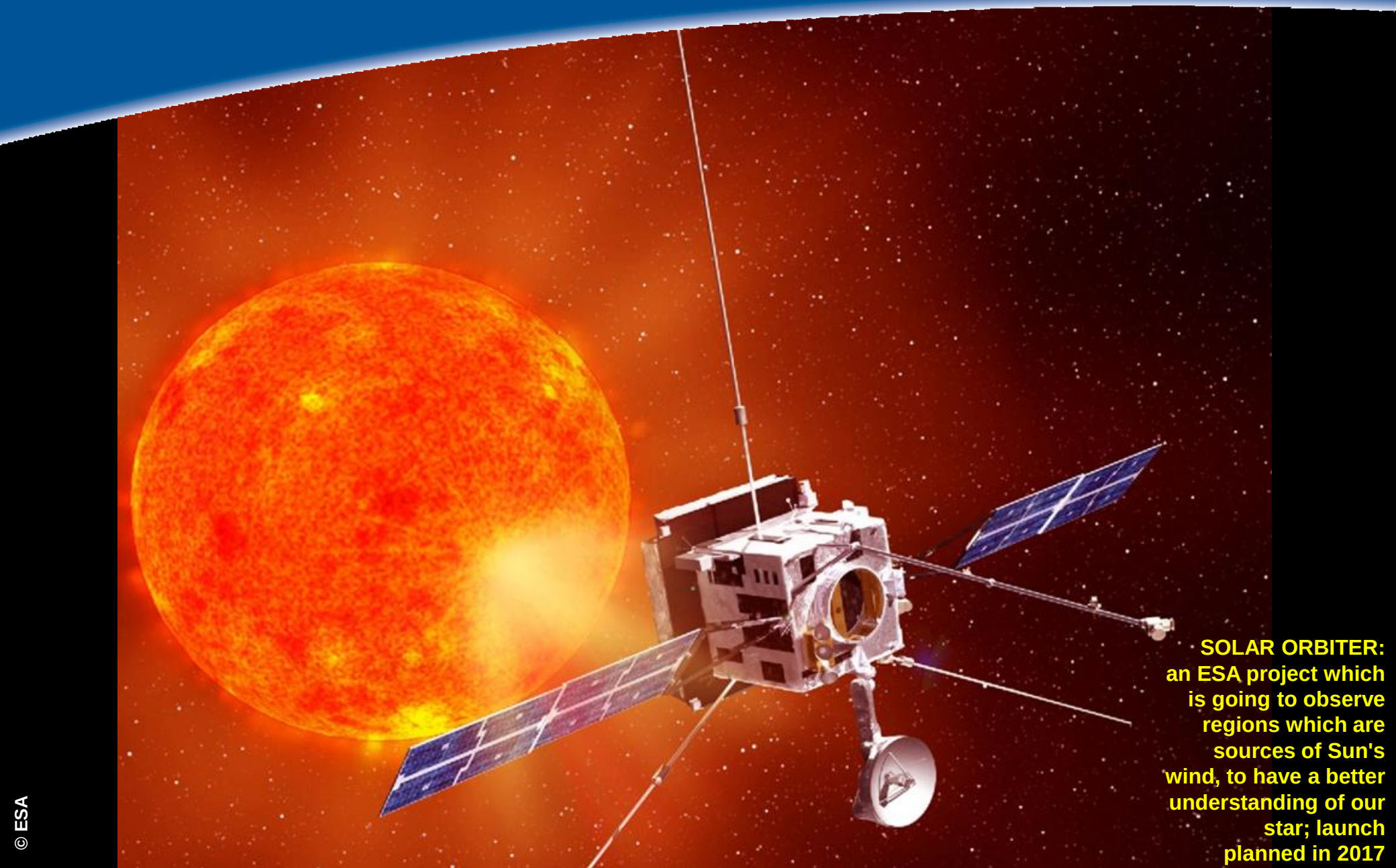
- If a COTS has to be qualified for a CNES project, its qualification must respect the rules of "RNC -> Product Assurance -> EEE components"

  EEE = Electrical, Electronic and Electro-mechanical

- For more information, please contact: normalisation@cnes.fr

- ECSS (European Cooperation for Space Standardization)

3 – Other difficulties linked with COTS ICs



SOLAR ORBITER:
an ESA project which is going to observe regions which are sources of Sun's wind, to have a better understanding of our star; launch planned in 2017

Bugs

- When manufacturers are aware of a bug in a HiRel component, users are generally notified
- This is not always the case with COTS => this can have serious impacts, financially and/or from a planning perspective

- G-Link result(s)
  - A bug was found in the G-Link Rx at a late stage of the Pleiades development, during a calibration test of the image chain based on the transmission of highly repetitive data
    - in 'Enhanced mode' (ESMPXENB pin to '1') the G-Link could become desynchronised; in 'Compatible mode' (ESMPXENB pin to '0'), the G-Link is stable and several hundred of Gbits were transmitted without error
  - Lot of characterization tests were done to unsuccessfully attempt to determine conditions which trig the bug to try to live with
    - unfortunately, some of these conditions were probably not fully deterministic…
    - … thus requiring to modify some FM (Flight Model) / EM (Engineering Model) / EGSE (Electrical Ground Support Equipment) units, incurring significant costs and delays

Turn-over cycle

- **Short life cycle of COTS wrt to a 5 - 8 years satellite life cycle**

- **G-Link result(s)**
  - **Thanks to the strategic stock, Pleiades was not disturbed by the evolution of the chip masks during the qualification step (the "A" new version, which has a higher power consumption); then by the obsolescence of the G-Link**
  - **Reuse capability: 8 projects use, or are going to use components from the G-Link qualified strategic stock**
    - **As a consequence, a "relifing test" (see next slide) was required due to the G-Link usage over a long period**
    - **The End-of-Life for the G-Link stock is 2012 => the G-Link stock is not usable anymore for space applications**

Use-by date of the qualified lot of components

- Not specific to COTS, but to the long term storage
- Nevertheless, COTS are more subject to (strategic stock)
  - LAT = authorisation to solder a lot of ICs for 7 years from the date-code
  - Relifing tests = authorisation to solder such lot for 3 more years
  - The lot cannot be used after this period of 7 + 3 years for space developments

  => Strategic storage should be accompanied by monitoring of aging of the stock, and regenerating it if required

  => Strategic storage is not a universal solution
- G-Link result(s)
  - The following relifing tests were successfully done
    - Verification of storage conditions conformity
    - External visual inspection of 100 'Tx + Rx' pairs => detection of bent pins on few parts (around 100 µm of misalignment) due to unsuitable carriers/boxes used during transports
    - DPA on 3 parts: soldering test, X rays, internal visual inspection, pull-test, depassivation and SEM (Scanning Electron Microscopy) inspection of the last metal layer, bond cratering
    - Electric tests of 80 'Tx + Rx' pairs at +25° C
    - HAST on 5 'Tx + Rx' pairs

SEU / SET sensitivity of COTS ICs

- All COTS are SEU / SET sensitive

  II
  V

- The use of COTS could require to mitigate SEU / SET
  - e.g. protection code for memories (EDAC), FT architectures for micro-processors, …

  II
  V

- Mitigation mechanisms and architectures have to be validated
  - e.g. FI (fault-injection), …

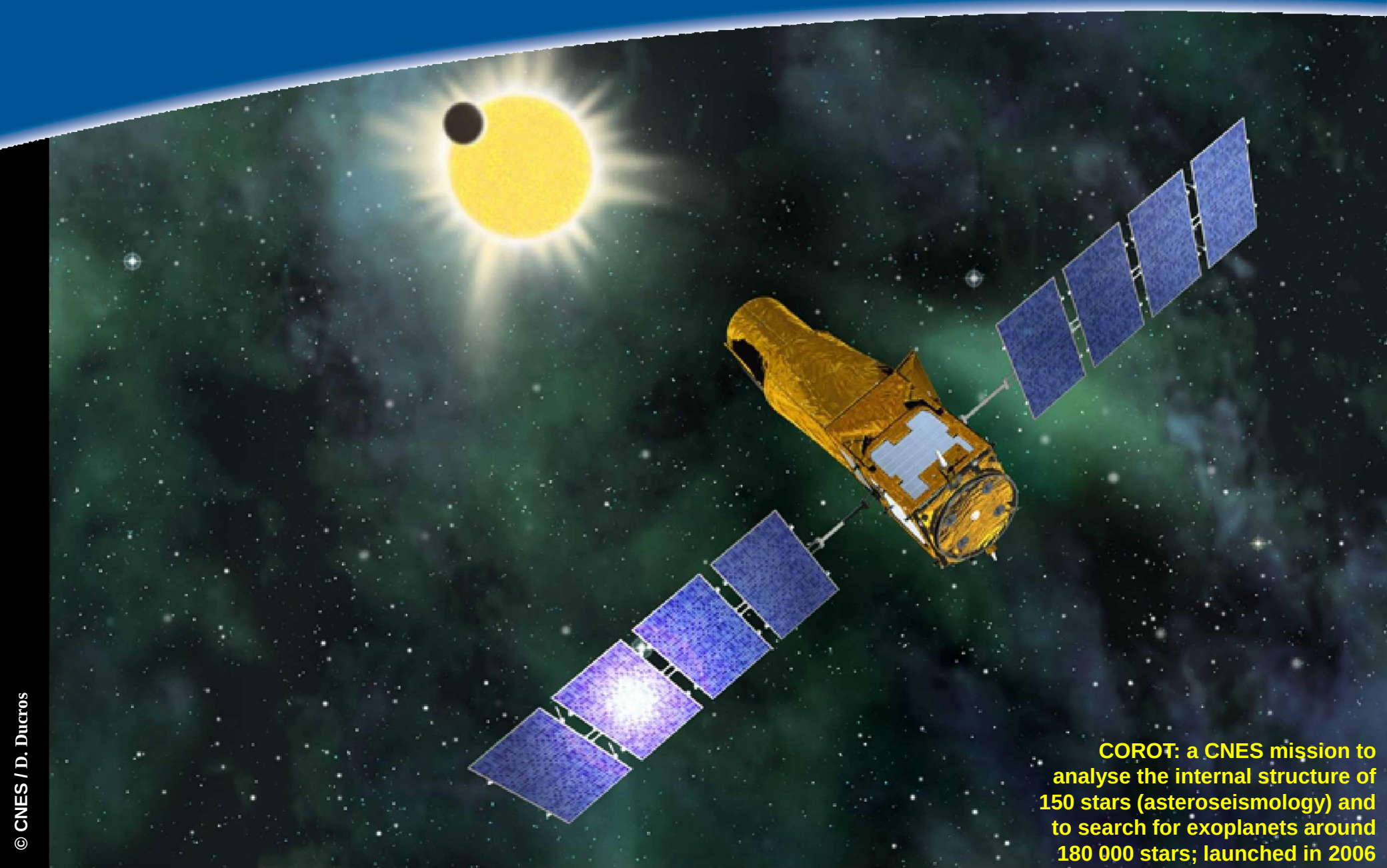
  II
  V

- So, wrt RadTol ICs, the use of COTS requires an additional function (SEU / SET mitigation => See "Software hardening" + "System hardening" talks), thus an extra 'validation work', it means extra cost / planning overheads

  II
  V

/!\ Validation of FT architectures could become a laborious work
=> pay attention to keep at a realistic and efficient level

4 – Limitations when using COTS ICs



COROT: a CNES mission to analyse the internal structure of 150 stars (asteroseismology) and to search for exoplanets around 180 000 stars; launched in 2006

Presentation of the COTS ICs performance limitations issue

- The high performances of COTS is the basis of their use in space

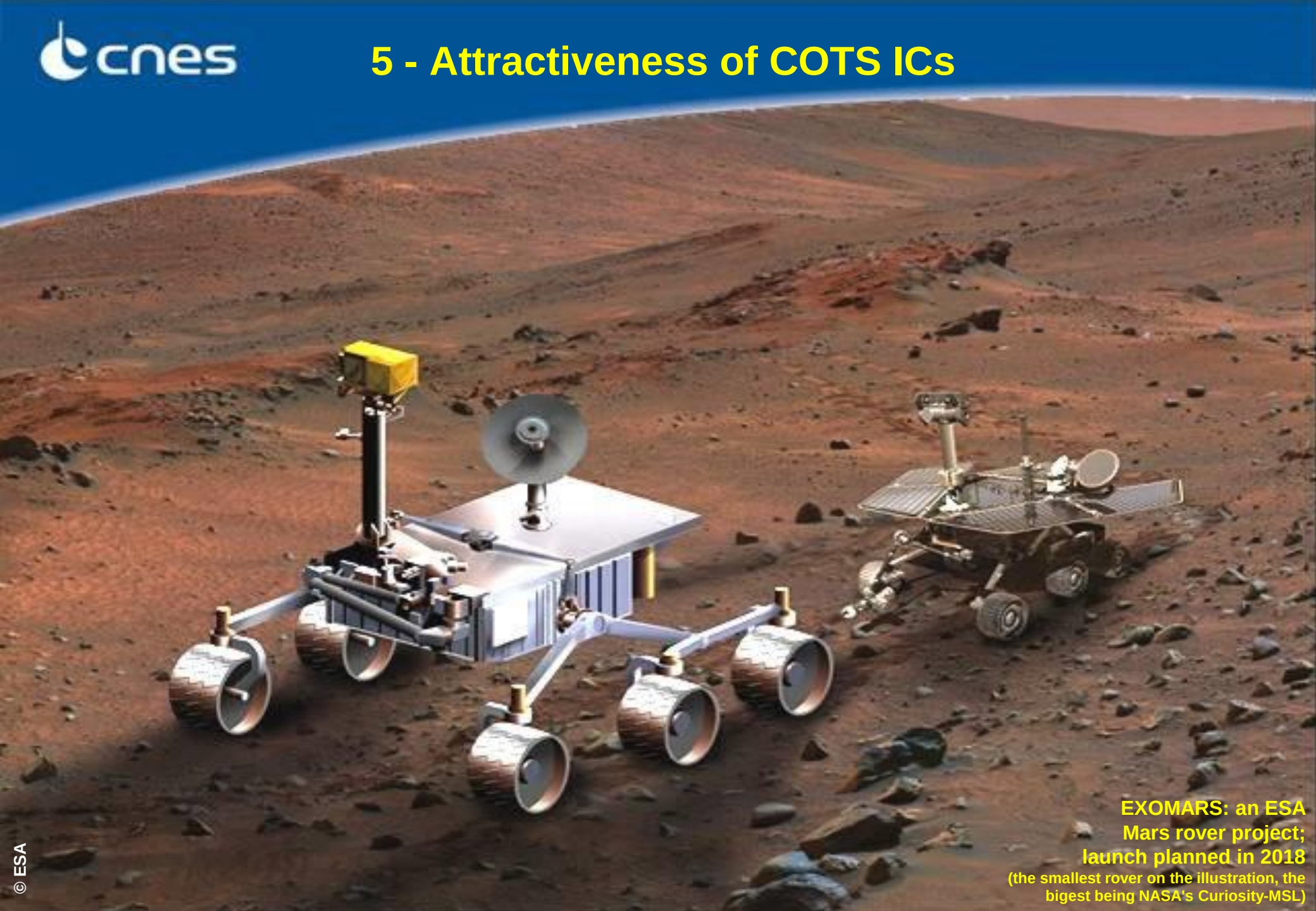
- But not all of these performances (not their full ranges), can be fully exploited in embedded applications, in particular in the space domain which cumulates:
  - harsh environment
    => the main constraint being radiation tolerance of components
  - impossibility to repair
    => strict rules for qualification of components
  - a very high cost per launched kilogramme
    => difficulties with e.g. HW replication architectures for ICs which have to be protected againts SEU
  - very low recurring production
    => which limits certain investments
  - application contraints
    (e.g. hard real-time constraints => difficulties with cache memories)

=> HW and SW designs must adapt the use of COTS to space constraints

Limitations concerning COTS ICs usable performances

- Functional and performance limitations will have to be taken into account for space applications
  - Reducing attractiveness of COTS
- Three examples
  - Bus frequency
  - Power consumption
  - Cache memories
- … among other constraints
  - Derating (e.g. 10 % margin on fan-in/fan-out, sometimes 10 % on clock frequency, ...)
  - Limitation on the number of usable gates with SRAM-based FPGA (Xilinx) due to the SEU mitigation mechanisms (TMR, …)
  - Limitation on the number of usable pins (see § "Mounting qualif" in Section 2)
  - etc.

5 - Attractiveness of COTS ICs



EXOMARS: an ESA Mars rover project; launch planned in 2018
(the smallest rover on the illustration, the bigest being NASA's Curiosity-MSL)

Attempt to provide trends
/!\ Be carefull with these values

Costs for a lot qualificat° of COTS ICs, for a space project having a quality level of the type of Pleiades (1/2)

	ICs simple to test (e.g. logic, memory)	ICs with medium complexity tests	ICs complex to test (e.g. SerDes, µP)
■ Selection	20 – 100 k€	20 – 200 k€	20 – 350 k€ -> 1.5 to 2.5 years
■ Procurement (α qty & IC price + ingeniery)	10 – 200 k€	10 – 200 k€	10 – 200 k€
■ Qualification (except ON-OFF tests)	50 – 100 k€ 0.75 year is the mini	100 – 150 k€	150 – 300 k€ -> 1.0 to 2.0 years
=> Total cost for a lot qualificat° of COTS	= 150 – 300 k€	= 300 – 500 k€	= 500 – 800 k€
■ Bug (α when the bug is detected)	0 – 300 k€	0 – 300 k€	0 – 300 k€ -> 1.0 years
■ Relifing	5 – 10 k€	10 – 20 k€	15 – 30 k€ 0.5 years
■ *On/Off tests* (very specific test, very hard to complete for G-Link)	*average 0.5 to 1 year*	*average 0.5 to 1 year*	*average 1 year* *worst-case 2 to 3 years*

Costs for a lot qualificat° of COTS ICs, for a space project having a quality level of the type of Pleiades (2/2)

- Global cost for an IC complex to test
  - Could be up to 1.0 M€ for a Pleiades-like quality level
  - Could range up from 1.0 M€ to 1.5 M€ for the highest quality level

- Competitiveness threshold for COTS wrt their space counterparts in a part-to-part replacement hypothesis
  - For 100 parts: space qualified ICs are cheaper
  - For 1000 parts: COTS ICs are cheaper…

    … but other factors are involved in the decision to qualify a COTS
    - risk
    - planning
    - etc.

Attractiveness of COTS ICs (1/2)

☹☹☹ ■ **The usage of COTS for space applications cumulates several difficulties**

- **Uncertainty to successfully pass all the qualification tests => high risk level**
- **High cost and planning overheads: selection, lot qualification tests, etc.**
- **Short life cycle wrt to a 5 - 8 years satellite development cycle**
- **Protections against SEU, specifically for COTS µP with FT archi. + validation by fault injection => high cost overheads (and planning if not anticipated through R&D)**
- **Full COTS performance not always reachable for a space project**

- **All these constraints reduce the attractiveness of COTS**
- **The 'cost of ownership' of COTS is potentially (far) higher than for their space qualified counterparts**

=> Are COTS components really attractive for the space domain?

Attractiveness (2/2)

CNES SSMM: 1st generation for Spot 4 (1995)

CNES HSSL: 1st gene. for Spot 5 (1997)

☺ ■ **Large quantity**: some rare ICs are used in very large quantity
=> compensate the COTS cost overhead

- Chip memories for SSMM (Solid State Mass Memories) → # 5 000 ICs
- HSSL (High Speed Serial Links) e.g. Agilent G-Link on Pleiades → # 1 000 ICs

☺ ■ **Unavailability** of some functions in space qualified grade

- Chip memories (mandatory for SSMM units): SDRAM, Flash NAND EEPROM
- Analog and mixed analog-digital ASIC technologies

☺ ■ **Feasibility** of space missions is sometimes linked to performances of COTS

- High performance commercial ADC for Earth observation image sensors
- High performance commercial DSP for missions as scientific ones
- High perfo commercial µP e.g. for some ambitious (scientific) missions as the GAIA one

=> Thanks to their high performances, COTS ICs are among technologies having a potential disruptive capability for future space missions

6 – Case studies at computer level

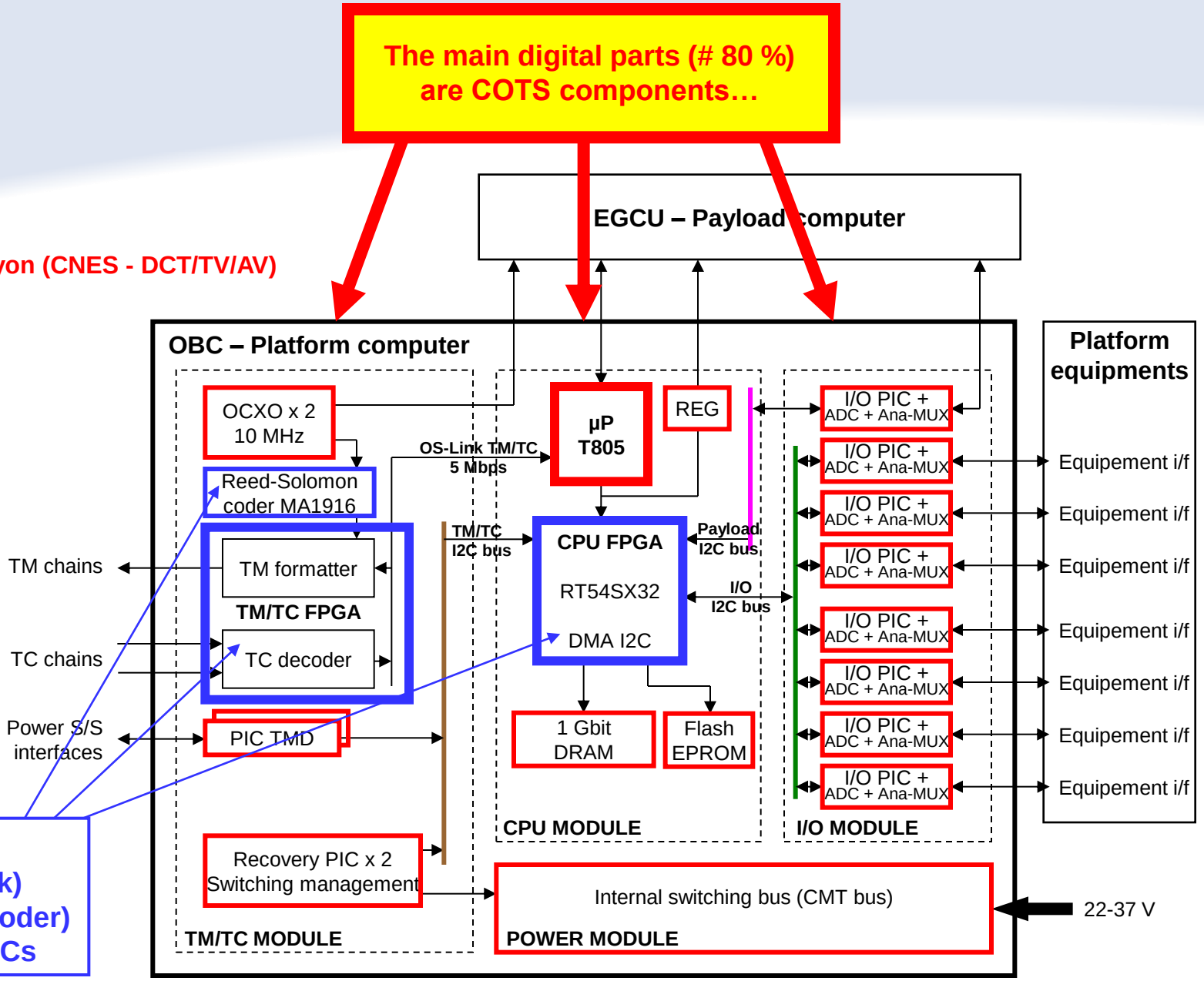
© ESA

GAIA: an ESA project (2030 kg) to generate the largest and most precise 3D map of our Galaxy; launched in 2013

MYRIADE

Contribution from: J-L. Carayon (CNES - DCT/TV/AV)

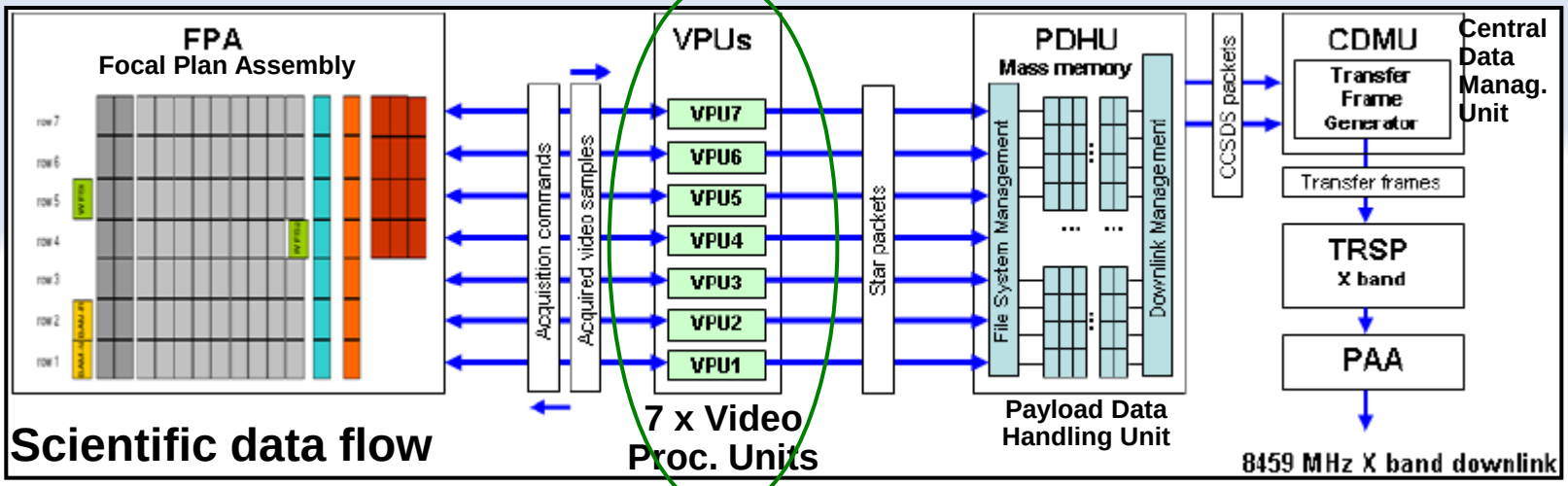
- CNES µsat
  - CNES design
  - Industrialisation by STEEL Electronique (SME)

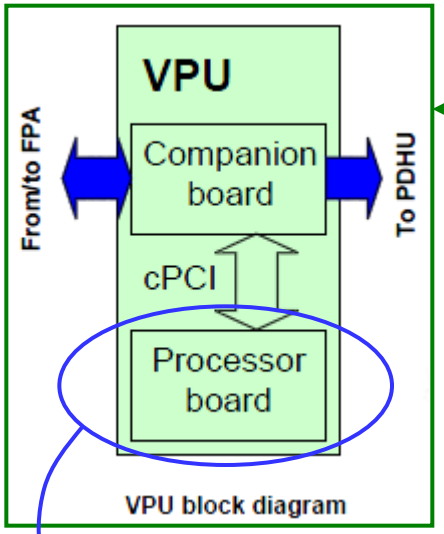


- The numerous mitigation mechanisms are presented in the talk "System Hardening"

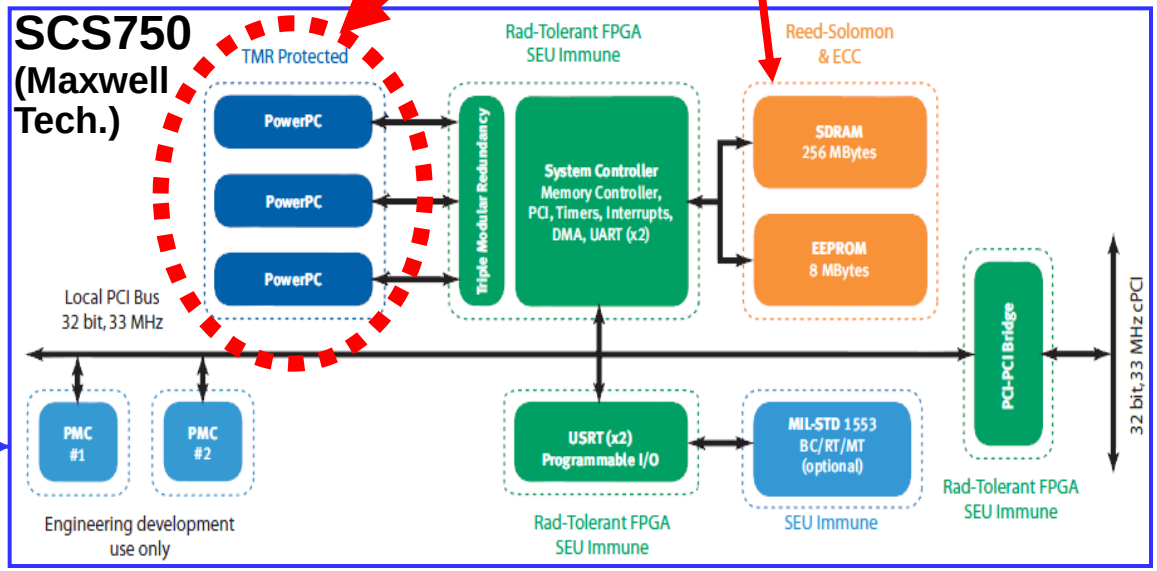
GAIA

- ESA large scientific mission
  - Prime = EADS Astrium





Mainly the µP *and memories* are COTS components



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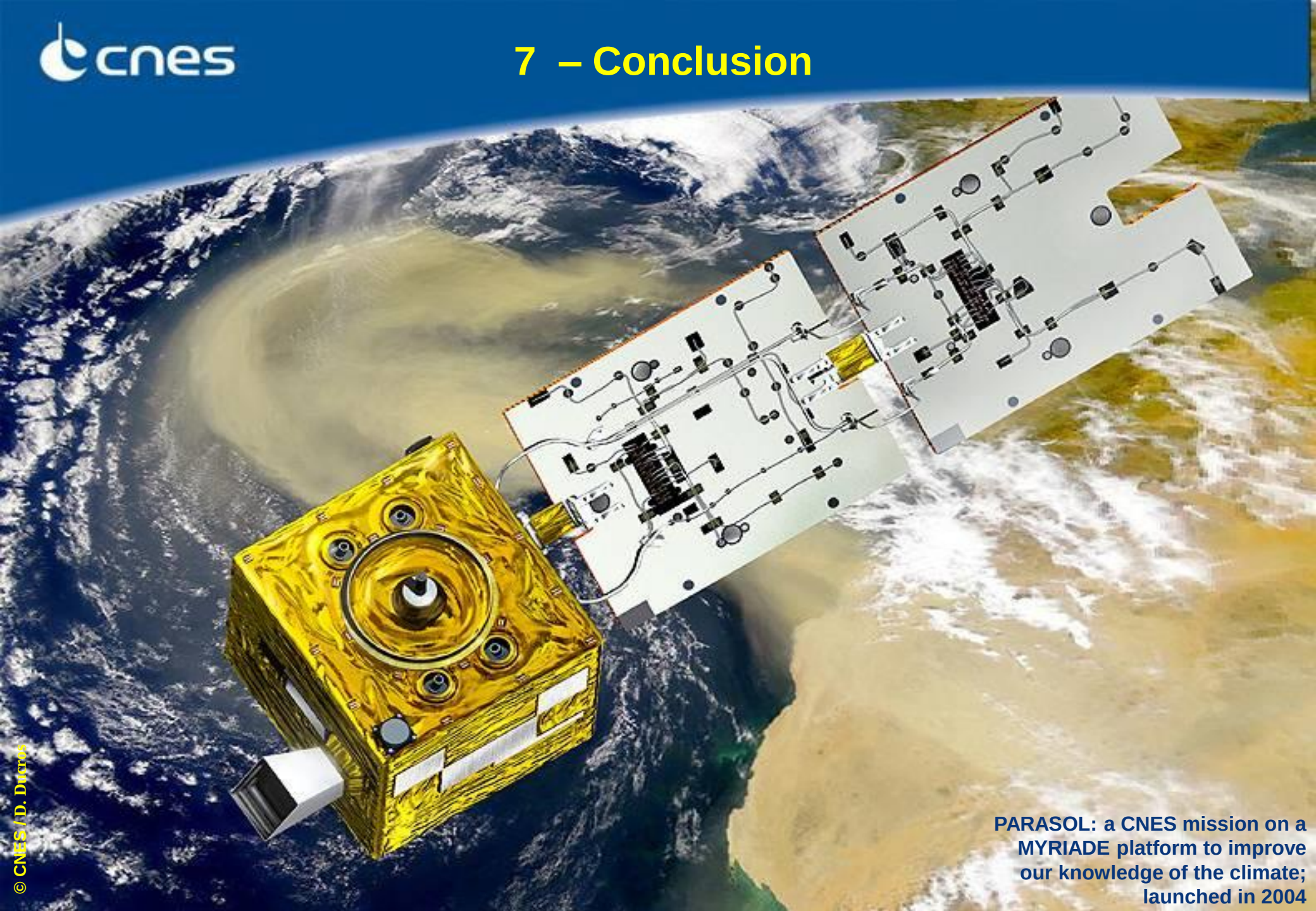
- The mitigation architecture for the µP is presented in the talk "System Hardening"

7 – Conclusion



PARASOL: a CNES mission on a MYRIADE platform to improve our knowledge of the climate; launched in 2004

Conclusion

- **The 'cost of ownership' of COTS ICs is potentially (far) higher than their space qualified counterparts => usually COTS are costly!**
  - **except for some rare components used in very large quantities**
  - **except for units and small satellites having a low quality level**

  => *only the contribution of COTS to system performance can justify their use in space avionics*

- **The uncertainty to succeed during the qualification steps (=> risk) and the qualification delay must be kept in mind**

- **COTS ICs are a disruptive technology, allowing the usage of spacecraft supercomputers**
  - **MYRIADE and GAIA are typical examples of the attractiveness of COTS… because without COTS ICs these missions would not be possible at their current performances**

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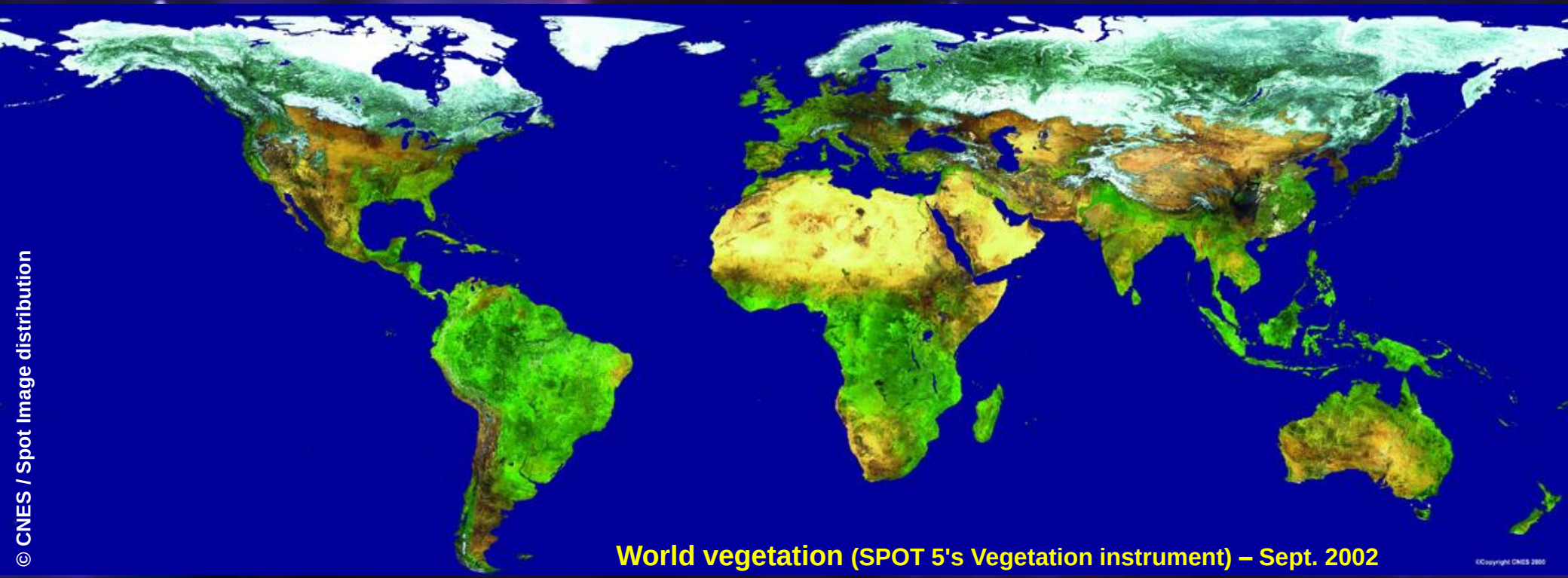
Gracias!
Thank you!



World vegetation (SPOT 5's Vegetation instrument) – Sept. 2002

Any questions?